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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/936,479	09/13/2001	Siegfried Schweidler	PD990014	6074

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Joseph S Tripoli
Thomson Multimedia Licensing
PO Box 5312
Princeton, NJ 08540

EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/936,479	SCHWEIDLER ET AL.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/13/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 7, 2005 has been entered.

Response to Amendment

2. This Office Action is in response to the amendment filed on January 14, 2004.

Information Disclosure Statement

3. The Information Disclosure Statement field on September 13, 2001 has been considered.

Claim Objections

4. Claim 5 is objected to because of the following informalities:

Claim 5, line 3 "a memory management device" should be --the management device-- because this limitation has been addressed in claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 8-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8-9 are depended on independent claim 1, however the independent claim 1 is a method claim, and claims 8-9 are apparatus claims which one skill in the art would not be understood whether the claimed limitation is directed to method or apparatus. Appropriate correction is required.

The following art rejections are applied from what is best understood of the claims in view of the 112 Second Paragraph problem list above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were

made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaka (US PAT 5,740,373) in view of Adachi et al. (US PAT. 6,115,425 hereinafter Adachi).

Regarding claim 1, Isaka discloses a method for the management of data received via a serial data bus (108) in a receiving device, i.e., package switching system (col. 4 line 29-44), comprising the steps of receiving data transmitted in bus packets having a variable length (col. 5 lines 25-31), the data being divided into data blocks having a defined length, a combination of a defined number n of data blocks, i.e., cell, forming a data source packet of fixed length, section-by-section transmission of the data source packet within the framework of data blocks being permitted, i.e., packet division unit (703, figure 7) incorporate with packet reconstruction unit (701, figure 7) divides the data into cells each having a fixed length and then outputs the cells to the transmit bus, and the packet reconstruction unit (701) further comprising a End-of-receipt Detect circuit (K1, figure 9) to detect the end of detection cell by cell, (col. 5 line 33 through col. 6 line 28), in addition, Isaka further teaches a last cell latch (802, figure 8) corresponding with the header information to determine the end of the data source packet transmission, and sends receive response data signal to the output device via bus (109) (col. 7 lines 25-52 and col. 9 line 36 through col. 10 line 7) and (col. 13 line 43 through col. 14 line 10). Isaka

differs from the claimed invention in not specifically teaches the steps of carrying out a modulo-n counting of the data blocks in order to determine the data source packet boundaries, and in that the beginning of a new data source packet is signaled to a memory management device at the beginning of the next counting interval. However, Adachi teaches a transmission device reorganize the variable length coded data, i.e., coded moving picture data, to have a pseudo fixed length via a control circuit (7, figure 1), fixing length circuit (9, figure 1), and buffer (6, figure 1) in the transmission device, in addition, Adachi teaches each of the variable length coded data blocks have a start point, and the start point is always located on the start point each pseudo fixed data block, so as the header and synchronization word to specify the specific group of data block, i.e., start point could be separated each of the data source packet boundaries, (col. 3 line 61 through col. 4 line 52, and col. 5 line 27 through col. 6 line 32), furthermore, Adachi teaches the way of calculating the data blocks in response to the code lengths of variable length coded data by the control circuit (col. 8 line 29-63 and col. 4 line 56 through col. 5 line 27), plus, Adachi further teaches a check word adding circuit (31, figure 5) in the transmission device wherein the check word adding circuit incorporate with the multiplexing/check word adding circuit (33, figure 5) having a predetermined constitution as required by calculation to a tail end of the output unit, so that the code length of a single output unit will be a multiple of a predetermined constant (col. 8 line 64 through col. 9 line 26). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method of the package switching system of Isaka in having a steps of carrying out a modulo-n counting of the data blocks in order to determine the data source packet boundaries, and in that the

beginning of a new data source packet is signaled to a memory management device at the beginning of the next counting interval, as per teaching by the transmission device of Adachi, because it reducing data losses occurrable due to code errors and a void an accidental bringing-out of information pertain.

Regarding claim 2, Isaka discloses each bus packet is subjected to CRC checking and the checking results are buffer-stored in order to be able to ascertain whether a data source packet transmitted in two or more bus packets has bee transmitted without transmission errors (col. 4 line 45 through col. 5 line 2).

Regarding claim 3, Isaka discloses a reference counter reading is transmitted in each bus packet in order to check the completeness of the transmitted data, and in which comparison counting of the received data blocks is effected and, when the data block associated with the reference counter reading is received, the result of the comparison counting is compared with the reference counter reading and an error signal is output in the event of non-correspondence, i.e., the packet reconstruction unit (701) comprising a End-of-receipt Detect circuit (K1, figure 9) to detect the end of detection cell by cell, (col. 5 line 33 through col. 6 line 28), a last cell latch (802, figure 8) corresponding with the header information to determine the end of the data source packet transmission, and sends receive response data signal to the output device via bus (109), (col. 7 lines 25-52 and col. 9 line 36 through col. 10 line 7) and (col. 13 line 43 through col. 14 line 10), when an error is detected during the course of receipt, and error/interrupt signal is sent back to the processor (706) (col. 9 line 37 through col. 12 line 8).

Regarding claim 4, the difference between Adachi and the claim is the claim specifically recites number n of data blocks of a data source packet corresponds to the

number 8 and the modulo-n counting is correspondingly modulo-8 counting. However, having the number 8 and modulo-8 counting do not have a disclosed purpose nor is it disclosed to overcome any deficiencies in the prior art. As such, the number n of data blocks of a data source packet corresponds may contain any number based on the manufacture required. In addition, Adachi teaches the way to dividing the variable length coded data into the pseudo fixed length blocks (col. 4 line 56 through col. 6 line 9), and the way to calculated the respectively data blocks for the incoming variable length moving picture coded data is vary (col. 8 lines 37-57 and col. 11 lines 31-43). Thus it would have been an obvious matter of design choice to utilize the counting way of Adachi, wherein the counting data blocks are variable which based on the variable length incoming data, as disclosed supra, since applicant has not disclosed that a number of 8 data blocks and modulo-8 counting, as opposed to other size, overcomes a deficiency in the prior art or is for any stated purpose.

Regarding claim 5, Adachi discloses the method for the management of the data further comprising a memory unit (6, figure 1) to which the received data are written in order, and having a memory management device, i.e., control circuit (7, figure 1) wherein a modulo-n counter is provided, which counts the received data blocks and outputs a data source packet start signal, i.e., start point, to the memory management device at the beginning of the next counting interval (col. 4 lines 6-52 and col. 5 line 27 through col. 6 line 32).

Regarding claims 6-7, the limitation of the claims are rejected as the same reasons set forth in claims 2-3.

Regarding claim 8, Adachi teaches discloses the method for the management of the data further comprising a counter, by which the data are counted in particular in units of bytes and which outputs a data block counting signal if the number of data that have been counted are as many as are defined as belonging to a data block (col. 4 line 56 through col. 6 line 9 and col. 8 line 37 through col. 9 line 26).

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaka (US PAT 5,740,373) and Adachi et al. (US PAT. 6,115,425 hereinafter Adachi) as applied to claim 1 above, and further in view of Hatae et al. (US PAT. 6,678,769 hereinafter Hatae).

Regarding claim 9, the combination of Isaka and Adachi differs from the claimed invention in not specifically teaches the method for the management of the data wherein the data bus is designed according to the IEEE 1394 standard and the apparatus is part of data link layer module in the interface for this data bus. However, Hatae teaches in the communication system (figure 1) comprising a source node, and destination node, and a controller (300, figure 1) for controlling data communication between the nodes by the transmission link, i.e., bus IEEE 1394-1995 with specific communication protocol (col. 7 line 9-54, col. 9 line 24 through col. 10 line 4, and col. 23 lines 29-59). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Isaka and Adachi in having the method for the management of the data wherein the data bus is designed according to the IEEE 1394 standard and the apparatus is part of data link layer module in the interface for this data bus, as per teaching by the communication system of Hatae, because it ensures a high speed to transmitting communication data in the network, and inhibiting an increase in a

delay time that occurs before data communication is initiated in the data communication network.

Response to Arguments

11. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sakamoto et al. (US PAT. 6,836,479) discloses variable length packet communication device (abstract).

Hammers et al. (US PAT. 6,608,839) discloses system and method for indicating an accurate committed information rate (abstract).

Aybay (US PAT. 6,185,221) discloses method and apparatus for fair and efficient scheduling of variable size data packets in an input-buffered multipoint switch (col. 3 line 28 through col. 6 line 26).

Cam et al. (US PAT. 6,671,758) discloses bus interface for cell and/or packet data transfer (col. 2 line 45 through col. 4 line 28).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183. The examiner can normally be reached on M-F 9:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

Patent Examiner
Art Unit 2186

MATTHEW D. ANDERSON
PRIMARY EXAMINER